What is Claimed is:

1. A method of forming in a semiconductor body of a first conductivity type in which there has been formed an array of memory cells which each comprise an insulated gate field effect transistor, which comprises first and second output regions of a second opposite conductivity type and a gate which is separated from the semiconductor body by a gate dielectric layer, contacts to the gates and the first output regions, the method comprising the steps of:

forming first insulating regions around portions of a top surface of the semiconductor body in which gate contacts are to be formed;

forming gate contacts using a Damascene process in the portions of the semiconductor body surrounded by the first insulating regions;

forming second insulating regions around exposed portions of the gate contacts;

forming a borderless contact to each one of the first output regions of each transistor with the first and second insulating regions electrically isolating the gate contacts from the contacts to the first output regions.

2. The method of claim 1 wherein the borderless contacts to the first output regions are formed using a Damascene process.

3. A method of forming in a semiconductor body, which has a top surface and being of a first conductivity type, and in which there has been formed an array of memory cells which each comprise a vertical insulated gate field effect transistor having first and second output regions of a second opposite conductivity type and a gate which is separated from a vertical surface of the semiconductor body by a gate dielectric layer, contacts to the gates and the first output regions, the method comprising the steps of:

forming vertical insulating regions around portions of the top surface of the semiconductor body in which gate contacts are to be formed;

forming gate contacts using a Damascene process in the portions of the semiconductor body surrounded by the first insulating regions;

forming horizontal insulating regions around exposed portions of the gate contacts;

forming a borderless contact to each one of the first output regions of each transistor with the vertical and horizontal insulating regions electrically isolating the gate contacts from the contacts to the first output regions.

4. The method of claim 3 wherein the borderless contacts to the first output regions are formed using a Damascene process.

5. A method of forming in a semiconductor body, which has a top surface and is of a first conductivity type, and in which there have been formed an array of memory cells which each comprise a trench capacitor and a vertical insulated gate field effect transistor, which comprises first and second output regions of a second opposite conductivity type and a gate which is separated from a vertical surface of the semiconductor body by a gate dielectric layer, electrical contacts to the gates and first output regions, the method comprising the steps of:

forming a first insulating layer over a top surface of the semiconductor body;

forming first openings through the first insulating layer so as to expose a portion of the top surface of the semiconductor body in which the gates are located;

forming insulating sidewall spacer regions on sidewalls of the openings through the first insulating layer with the insulating sidewall spacer regions being of a different material than the first insulating layer;

over filling the first openings through the first insulating layer with a first conductor which contacts the gates of each transistor and extends over a top surface of the first insulating layer;

removing portions of the first conductor on the top surface of the first insulating layer so as to result in a segmented first conductor filling each of the first openings;

covering exposed surfaces of the first conductors with a second insulating layer which is of a material different than that of the first insulating layer;

forming first openings through the second insulating layer and second openings through the first insulating layer between adjacent insulating sidewall spacer regions to expose portions of the semiconductor top surface which include portions of the first output regions; and

filling each of the second openings through the first insulating layer with a second conductor which contacts a first output region such that each second conductor is self aligned and borderless.

6. A method of forming in a semiconductor body of a first conductivity type in which there have been formed an array of memory cells which each comprise a trench capacitor and a vertical insulated gate field effect transistor, which comprises first and second output regions of a second opposite conductivity type and a gate which is separated from a surface of the semiconductor body by a gate dielectric layer, electrical contacts to the gate and first output region, the method comprising the steps of:

forming a first insulating layer over a top surface of the semiconductor body;

forming separated first openings through the first insulating layer so as to expose a portion of the top surface of the semiconductor body in which the gates are located;

forming insulating sidewall spacer regions on sidewalls of the openings through the first insulating layer with the insulating sidewall spacer regions being of a different material than the first insulating layer;

over filling the first openings through the first insulating layer with a first conductor which contacts the gates of each transistor and extends over a top surface of the first insulating layer;

removing portions of the first conductor on the top surface of the first insulating layer so as to result in a segmented first conductor filling each of the first openings;

removing portions of the segmented first conductors so as to recess same in each of the first openings;

over filling the first openings with a second insulating layer which is of a material different than that of the first insulating layer;

removing portions of the second insulating layer so as to form a planar surface which includes portions of the first and second insulating layers;

forming second openings through the first insulating layer between adjacent insulating sidewall spacer regions to expose portions of the semiconductor top surface which include portions of the first output regions; and

filling each of the second openings through the first insulating layer with a second conductor which contacts a first output region such that each second conductor is self aligned and borderless.

7. The method of claim 6 wherein:

each of the second openings is over filled with a second conductor; and

removing portions of the second conductor which overfills the second openings so as to form separated second conductors which each contact a first output region.

8. The method of claim 7 wherein the removing of portions of the first and second conductors is done using chemical mechanical polishing.

9. The method of claim 7 wherein the removing of portions of the first and second conductors is done chemical etching.

10. The method of claim 6 wherein the first insulating layer is silicon oxide and the second insulating layer is silicon nitride.

11. The method of claim 7 wherein the removing of portions of the first and second conductors is done using chemical mechanical polishing.

12. The method of claim 7 wherein the removing of portions of the first and second conductors is done chemical etching.

13. The method of claim 6 wherein the first insulating layer is silicon oxide and the second insulating layer is silicon nitride.

14. A method of forming in a semiconductor body of a first conductivity type in which there have been formed an array of memory cells which each comprise a trench capacitor and a vertical insulated gate field effect transistor, which comprises first and second output regions of a second opposite conductivity type and a gate which is separated from a surface of the semiconductor body by a gate dielectric layer, electrical contacts to the gate and first output region, the method comprising the steps of:

forming a first insulating layer over a top surface of the semiconductor body;

forming separated first openings through the first insulating layer so as to expose a portion of the top surface of the semiconductor body in which the gates are located;

forming insulating sidewall spacer regions on sidewalls of the openings through the first insulating layer with the insulating sidewall spacer regions being of a different material than the first insulating layer;

over filling the first openings through the first insulating layer with a first conductor which contacts the gates of each transistor and extends over a top surface of the first insulating layer;

removing portions of the first conductor on the top surface of the first insulating layer so as to result in a segmented first conductor filling each of the first openings;

removing portions of the segmented first conductors so as to recess same in each of the first openings;

over filling the first openings with a second conformal insulating layer which is of a material different than that of the first insulating layer;

filling recesses in the second conformal insulating layer with a self planarizing third insulator layer so as to form a planar surface common to the second conformal insulating layer and the self planarizing insulator layer, the self planarizing insulator layer being of a different material than the first insulating layer;

removing portions of the second conformal insulating layer not covered by the self planarizing third insulating layer;

removing the self planarizing third insulator layer;

forming a fourth insulating layer over the resulting structure;

removing all portions of the fourth insulating layer except those portions which are over the remaining portions of the second insulating layer and remaining portions of the first insulator layer to create separated first openings through the fourth insulator layer and second openings through the first insulator layer to expose portions of the top surface of the semiconductor body in which are located the first output regions, the first openings through the fourth insulating layer and the second openings through the first insulating layer being aligned;

filling each of the first openings through the fourth insulating layer and the second openings through the first insulating layer with a second conductor which contacts a first output region such that each second conductor is self aligned and borderless.

15. The method of claim 14 wherein:

each of the first openings in the fourth insulating layer is overfilled with the second conductor; and

removing portions of the second conductor which overfills the first openings in the fourth insulating layer so as to form separated second conductors which each contact a first output region.

16. The method of claim 14 wherein the removing of portions of the first and second conductors is done using chemical mechanical polishing.

17. The method of claim 14 wherein the removing of portions of the first and second conductors is done chemical etching.

18. The method of claim 14 wherein the first insulating layer is silicon oxide, the second insulating layer is silicon nitride, the self planarizing third insulator layer is chosen from a group consisting of an anti-reflective material and polysilicon, and the fourth insulating layer is boron phosphosilicate glass.